Application for
UNITED STATES LETTERS PATENT

Of

SATOSHI SUGAHARA

AND

MASAAKI TANAKA

FOR

A SPIN TRANSISTOR BASED ON THE SPIN-FILTER EFFECT AND A NONVOLATILE MEMORY USING SPIN TRANSISTORS

SPECIFICATION

A SPIN TRANSISTOR BASED ON THE SPIN-FILTER EFFECT AND A NONVOLATILE MEMORY USING SPIN TRANSISTORS

TECHNICAL FIELD

The present invention relates to a novel transistor. More specifically, the present invention relates to a transistor having an output characteristic depending on the direction of the spin of carriers and a nonvolatile memory circuit (nonvolatile memory) using the same.

BACKGROUND ART

As a semiconductor memory used in electronic equipment typified by a microcomputer, a DRAM (Dynamic Random Access Memory) has been mainly used from the viewpoint of operating speed and integration. In the DRAM, it is difficult to respond to a request to save energy and mobile equipment in recent years due to the problems that energy is consumed for holding memory and the stored contents are lost when turning off the power. To respond to such request, essential is a novel memory having a nonvolatile characteristic in addition to high-speed, high integration and low power consumption characteristics.

Attention is being focused on an MRAM (Magnetoresistive Random Access Memory) as a next-generation memory which can realize operating speed and integration equal to those of the DRAM and has a nonvolatile characteristic. The MRAM stores information according to the directions of magnetization of ferromagnetic substances and electrically reads the information according to the

directions of magnetization by the giant magnetoresistance effect of a spin valve device or the tunneling magnetoresistance (TMR) effect of a magnetic tunnel junction (MTJ). The MRAM which uses the ferromagnetic substances can hold information in nonvolatile manner without consuming energy.

FIGS. 17(A) and 17(B) are diagrams showing a typical cell structure of an MRAM using an MTJ. As shown in FIG. 17(A), in the MRAM, a one-bit memory cell is constituted by one MTJ and one MOS (Metal Oxide Semiconductor) transistor. The gate of the MOS transistor is connected to a read word line, the source thereof is grounded, the drain thereof is connected to one end of the MTJ, and the other end of the MTJ is connected to a bit line.

As shown in FIG. 17(B), the MTJ has a tunnel junction structure having a thin insulator film interposed between two ferromagnetic electrodes and has the TMR effect in which tunnel resistance is different according to the relative directions of magnetization of the two ferromagnetic electrodes. In particular, the rates of change of the TMR when the two ferromagnetic electrodes have parallel magnetization and when they have anti-parallel magnetization are called a TMR ratio which is used for evaluating the TMR effect.

The MRAM stores information by allowing the magnetization state of the MTJ, that is, the relative directions of magnetization of the two ferromagnetic electrodes to be parallel magnetization or anti-parallel magnetization by a synthesized magnetic field induced by electric currents flowed to a bit line and a rewrite word line, not shown, orthogonal thereto.

To read stored information stored in a specified cell, a voltage is applied to a specified read word line connected to the cell to conduct the MOS transistor, a read electric current (hereinafter,

called a "driving current") is flowed from a specified bit line connected to the cell to the MTJ, and the voltage drop of the MTJ based on the TMR effect is detected as an output voltage to read the stored information.

DISCLOSURE OF THE INVENTION

The MRAM using the MTJ employs the ferromagnetic substances to have nonvolatile, low power consumption, and high-speed characteristics. The cell structure is simplified to be suitable for high density integration. The MRAM is expected as a next-generation nonvolatile memory. To realize this, there are the following problems to be solved.

(1) The MTJ has a binary resistance value corresponding to the magnetization states of parallel magnetization and anti-parallel magnetization. The MRAM flows the driving current to the MTJ to detect the resistance value as an output voltage. To obtain a high output voltage, the thickness of the insulator film of the MTJ must be adjusted to optimize the tunnel resistance. Since the TMR ratio depends on the thickness of the insulator film, optimizing the tunnel resistance is limited.

(2) To precisely read the memory contents of information, the TMR ratio must be large to increase the ratio of the output voltages of two magnetization states of parallel magnetization and anti-parallel magnetization. To realize a high TMR ratio, ferromagnetic substances having large spin polarizability must be used to optimize the forming method, material and film thickness of the insulator layer.

(3) In the MRAM using the MTJ, a bias applied to the MTJ must be large to increase the operating speed. The MTJ has an unavoidable

problem in principle that the TMR ratio is decreased when the voltage drop caused between the ferromagnetic electrodes is increased. The rate of change of an output voltage based on the TMR is decreased as the voltage drop caused in the MTJ is increased. The phenomenon is due to the TMR effect itself. It is difficult to avoid it as long as the magnetization states are read only based on the TMR effect.

Summarizing the above problems, to detect stored information with high sensitivity in the MTJ, the impedance (junction resistance) of the MTJ must be adjusted to optimize the magnitude of output voltages. Further, the TMR ratio must be large to increase the ratio of the output signals of two magnetization states of parallel magnetization and anti-parallel magnetization. The bias resistance of the TMR ratio is necessary so as not to decrease the TMR ratio by a bias.

If an output signal can be freely designed by the peripheral circuits other than a storage device regardless of the characteristic of the storage device, all the above problems can be solved.

An object of the present invention is to provide a nonvolatile memory which stores information in ferromagnetic substances included in a transistor according to a magnetization state and reads the information using an output characteristic of the transistor depending on the direction of the spin of carriers.

According to one viewpoint of the present invention, there is provided a transistor having a spin injector injecting spin-polarized hot carriers by a spin filter effect and a spin analyzer for selecting the injected spin-polarized hot carriers by the spin filter effect. The output characteristic of the transistor can be controlled depending on the direction of the spin of the spin-polarized hot carriers.

Preferably, the spin injector has a first ferromagnetic barrier layer, a first nonmagnetic electrode layer joined to one end surface of the first ferromagnetic barrier layer, and a second nonmagnetic electrode layer joined to the other end surface of the first ferromagnetic barrier layer.

Preferably, the spin analyzer has a second ferromagnetic barrier layer, the second nonmagnetic electrode layer joined to one end surface of the second ferromagnetic barrier layer, and a third nonmagnetic electrode layer joined to the other end surface of the second ferromagnetic barrier layer, and shares the second nonmagnetic electrode layer with the spin injector.

Preferably, the first and second ferromagnetic barrier layers include an insulating ferromagnetic semiconductor or a ferromagnetic insulator, and the energy band edges of the ferromagnetic barrier layers are constituted by any one of an up spin band and a down spin band by the spin split. Preferably, the thickness of the second nonmagnetic electrode layer is below the mean free path of the spin-polarized hot carriers of the second nonmagnetic electrode layer.

The spin injector has a large tunnel probability to carriers having a spin parallel to the spin band constituting the band edge of the first ferromagnetic barrier layer and a small tunnel probability to carriers having a spin anti-parallel thereto. The carriers having a spin parallel to the spin band constituting the band edge of the first ferromagnetic barrier layer can be injected as hot carriers from the first nonmagnetic electrode into the second nonmagnetic electrode layer.

The spin analyzer conducts, by the spin split at the band edge of the second ferromagnetic barrier layer, the spin-polarized hot

carriers to the third nonmagnetic electrode layer when the direction of the spin of the spin-polarized hot carriers injected into the second nonmagnetic electrode is parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer and does not conduct the spin-polarized hot carriers to the third ferromagnetic electrode when the direction of the spin-polarized hot carriers is anti-parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer.

The output characteristic of the transistor under the same bias depends on the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer. When the first ferromagnetic barrier layer and the second ferromagnetic barrier layer have parallel magnetization, a current transmission factor or a current amplification factor is high. When they have anti-parallel magnetization, a current transmission factor or a current amplification factor is low.

There is provided a nonvolatile memory circuit which stores information according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer and reads the information based on the output characteristic of the transistor depending on the magnetization state. The memory circuit can constitute a memory cell by the transistor alone.

According to another aspect of the present invention, there is provided a nonvolatile memory circuit having means storing information according to the directions of magnetization of ferromagnetic substances using a spin transistor including the ferromagnetic substances having an output characteristic depending on the direction of the spin of carriers, and means electrically reading

the information stored in the spin transistor from the output characteristic.

Preferably, the spin transistor has at least one ferromagnetic substance (hereinafter, called a "free layer") capable of independently controlling the direction of magnetization and at least one ferromagnetic substance (hereinafter, called a "pin layer") not changing the direction of magnetization, and holds, as stored information, a first state in which the direction of magnetization of the free layer is the same as the direction of magnetization of the pin layer and a second state in which the directions of magnetization are different.

Preferably, the spin transistor has a first electrode structure injecting spin-polarized carriers, a second electrode structure receiving the spin-polarized carriers, and a third electrode structure controlling the quantity of the spin-polarized carriers conducted from the first electrode structure to the second electrode structure, and the pin layer and the free layer are included in any one of the first to third electrode structures.

There is provided a storage circuit having a spin transistor arrayed in matrix, a word line connected to the third electrode structure, a first wire grounding the first electrode structure, and a bit line connected to the second electrode structure. A plurality of word lines are extended in the column direction. Multiple bit lines are extended in the direction crossing the same (the row direction). The spin transistor is arrayed near the cross point of the word line and the bit line.

The memory circuit inverts the magnetization of the free layer by magnetic fields induced by flowing electric currents to a first another wire and a second another wire crossing in the state of being

electrically insulated from each other on the spin transistor to change the relative magnetization state of the free layer and the pin layer for storing (or rewriting) information.

In place of the first another wire and the second another wire or any one of the first another wire and the second another wire, the word line and the bit line can be used or any one of the word line and the bit line can be used.

The memory circuit can read information based on the output characteristic of the spin transistor when the free layer and the pin layer included in the spin transistor have parallel magnetization.

There is provided the memory circuit in which an output terminal is formed at one end of each of the bit lines and a second wire branched from each of the bit lines and connected via a load to a power source is provided.

In this case, information can be read by an output voltage obtained based on the voltage drop of the load by an electric current produced between the first and second electrode structures of the spin transistor depending on the relative magnetization state of the free layer and the pin layer.

Using the above circuit can provide a high-speed nonvolatile memory circuit with high integration density which can design an output voltage according to a magnetization state in the transistor by a load and a power source.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(A) and 1(B) are diagrams showing the structure of a spin filter transistor according to this embodiment, in which FIG. 1(A) is a schematic cross-sectional view and FIG. 1(B) is an energy band diagram of conduction bands (or valence bands) of the structure

shown in FIG. 1(A) with the directions of the spins of the spin bands of barrier layers;

FIGS. 2(A) and 2(B) are energy band diagrams when applying base ground bias voltages between the emitter (a first nonmagnetic electrode layer), the base (a second nonmagnetic electrode layer), and the collector (a third nonmagnetic electrode layer) of the spin filter transistor according to this embodiment, in which FIG. 2(A) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are parallel to each other and FIG. 2(B) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are anti-parallel to each other;

FIGS. 3(A) and 3(B) are diagrams showing a static characteristic in the base ground of the spin filter transistor according to this embodiment in which the horizontal axis indicates collector-base voltage V_{CB} in the right direction in the drawing and emitter-base voltage V_{EB} in the left direction therein and the vertical axis indicates emitter current I_E, base current I_B, and collector current I_C, in which FIG. 3(A) shows a characteristic of the case that the magnetization state between the ferromagnetic barrier layers of the emitter and the collector is parallel magnetization and FIG. 3(B) shows a characteristic of the case that it is anti-parallel magnetization;

FIG. 4(A) is a diagram showing a structural example of memory cells using spin filter transistors 1 according to this embodiment, FIG. 4(B) is a diagram showing a structural example of a memory circuit, and FIG. 4(C) is a diagram in which the vertical axis indicates collector current I_C, the horizontal axis indicates collector-emitter voltage V_{CE}, and an I_C-V_{CE} characteristic of spin filter transistors 1

and a load straight line by a load resistance are shown in the same drawing;

FIG. 5(A) is a diagram schematically showing an example of an output characteristic of a current-driven type spin transistor, and FIG. 5(B) is a diagram schematically showing an example of an output characteristic of a voltage-driven type spin transistor;

FIG. 6(A) is a diagram showing a structural example of memory cells using voltage-driven type spin transistors according to this embodiment, FIG. 6(B) is a diagram showing a structural example of a memory circuit, and FIG. 6(C) is a diagram in which the vertical axis indicates drain current I_D, the horizontal axis indicates drain-source voltage V_{DS}, and an I_D-V_{DS} characteristic of voltage-driven type spin transistors 150 and a load curve by active load are shown in the same drawing;

FIG. 7 is an energy band diagram showing a structural example of a hot electron transistor type spin transistor;

FIG. 8 is an energy band diagram showing a structural example of a hot electron transistor type spin transistor using heat release injection;

FIG. 9 is an energy band diagram showing a structural example of a hot electron transistor type spin transistor using a spin filter effect;

FIG. 10 is an energy band diagram showing a structural example of a tunnel base transistor type spin transistor;

FIG. 11 is a cross-sectional view showing a structural example of a MOS transistor type spin transistor;

FIG. 12 is a cross-sectional view showing a structural example of a modulation dope transistor type spin transistor;

FIG. 13 is a cross-sectional view showing a structural example of a MOS transistor type spin transistor having a ferromagnetic semiconductor channel;

FIG. 14 is a cross-sectional view showing a structural example of a spin transistor having a structure in which a gate insulator film and a gate electrode are provided to a nonmagnetic insulating tunnel barrier provided between a ferromagnetic source and a ferromagnetic drain;

FIG. 15 is a cross-sectional view showing a structural example of a spin transistor having a structure in which a gate insulator film and a gate electrode are provided to an insulating ferromagnetic tunnel barrier provided between a ferromagnetic source and a ferromagnetic drain or a nonmagnetic drain;

FIG. 16(A) is a diagram showing a structural example of memory cells having a shared source structure;

FIG. 16(B) is a diagram showing a cross-sectional structure example of the memory cells having a shared source structure; and

FIG. 17(A) is a diagram showing the structure of a typical MRAM using an MTJ, and FIG. 17(B) is a diagram showing the operating principle of the MTJ.

BEST MODE FOR CARRYING OUT THE INVENTION

A transistor according to the present invention has a spin injector injecting spin-polarized hot carriers having the direction of a specified spin, and a spin analyzer selecting the injected spin-polarized hot carriers according to the direction of the spin. The spin injector has a first ferromagnetic barrier layer having a thickness permitting a tunnel effect such as Fowler-Nordheim tunnel or direct tunnel, a first nonmagnetic electrode layer joined to one end surface

of the first ferromagnetic barrier layer, and a second nonmagnetic electrode layer joined to the other end surface of the first ferromagnetic barrier layer. The spin analyzer has a second ferromagnetic barrier layer, a second nonmagnetic electrode layer joined to one end surface of the second ferromagnetic barrier layer, and a third nonmagnetic electrode layer joined to the other end surface of the second ferromagnetic barrier layer, and shares the second nonmagnetic electrode layer with the spin injector. The thickness of the second nonmagnetic electrode layer is preferably below the mean free path of the spin–polarized hot carriers of the nonmagnetic electrode layer.

The above structure is compared with the structure of a known hot electron transistor. The first nonmagnetic electrode layer and the first ferromagnetic barrier layer correspond to an emitter and an emitter barrier. The second nonmagnetic electrode layer corresponds to a base. The second ferromagnetic barrier layer and the nonmagnetic electrode layer correspond to a collector barrier and a collector.

The first and second ferromagnetic barrier layers include an insulating ferromagnetic semiconductor or a ferromagnetic insulator. The energy bands of the ferromagnetic barrier layers are spin split by magnetic exchange interaction. Only an up spin band or only a down spin band exist at the band edges by the spin split. The energy width in which only one of the spin bands exists is called a spin split width.

According to the spin filter effect of the spin injector, in the tunnel effect such as Fowler–Nordheim (FN) tunnel or direct tunnel produced by applying a voltage via the first nonmagnetic electrode layer and the second nonmagnetic electrode layer to the first ferromagnetic barrier layer, large is the tunnel probability of the carriers having the direction of the spin (when the carriers are

electrons, referring to the direction of the spin anti–parallel to the magnetization of the first ferromagnetic barrier layer, and when the carriers are holes, referring to the spin parallel to the magnetization of the first ferromagnetic barrier layer) matched with the direction of the spin of the spin band at the band edge of the first ferromagnetic barrier layer of the carriers of the first nonmagnetic electrode layer, and small is the tunnel probability of the carriers having the direction of the spin (when the carriers are electrons, referring to the direction of the spin parallel to the magnetization of the first ferromagnetic barrier layer, and when the carriers are holes, referring to the spin anti–parallel to the magnetization of the first ferromagnetic barrier layer) not matched therewith.

According to the spin filter effect of the spin analyzer, in the case of injecting spin–polarized hot carriers from the spin injector into the spin split band of the second ferromagnetic barrier layer, when the direction of the spin of the injected spin–polarized hot carriers is parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer (the first and second ferromagnetic barrier layers have parallel magnetization), the spin–polarized hot carriers are conducted through the spin band of the second ferromagnetic layer to the third nonmagnetic electrode layer, and when the direction of the spin of the spin–polarized hot carriers is anti–parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer (the first and second ferromagnetic barrier layers have anti–parallel magnetization), the spin–polarized hot carriers cannot be conducted through the second ferromagnetic barrier layer.

According to the above structure, the carriers in the first nonmagnetic electrode layer having the direction of the spin parallel

to the direction of the spin of the spin band at the band edge of the first ferromagnetic barrier layer are injected as spin-polarized hot carriers into the second nonmagnetic electrode layer by the tunnel effect such as Fowler-Nordheim tunnel or direct tunnel. At this time, the above transistor is biased so that the energy of the injected spin-polarized hot carriers is larger than the energy at the spin band edge at the band edge of the second ferromagnetic barrier layer and is smaller than the energy in which the spin split width is applied to the spin band edge. The thickness of the second nonmagnetic electrode layer is below the mean free path of the spin-polarized hot carriers in the second nonmagnetic electrode layer. The injected spin-polarized hot carriers reach the second ferromagnetic barrier layer without losing energy. The energy of the spin-polarized hot carriers is larger than the energy of the spin band edge at the band edge of the second ferromagnetic barrier layer and is smaller than the energy in which the spin split width is added to the spin band edge. When the direction of the spin of the injected spin-polarized hot carriers is parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer, the spin-polarized hot carriers are conducted through the spin band by an electric field produced in the second ferromagnetic barrier layer, are carried to the third nonmagnetic electrode layer, and become an electric current flowing between the third nonmagnetic electrode layer and the first nonmagnetic electrode layer.

When the direction of the spin of the injected spin-polarized hot carriers is anti-parallel to the direction of the spin of the spin band at the band edge of the second ferromagnetic barrier layer, the spin-polarized hot carriers are scattered (or backscattered) at the interface of the second nonmagnetic electrode layer and the second

ferromagnetic barrier layer, and become an electric current flowing between the second nonmagnetic electrode layer and the first nonmagnetic electrode layer.

Depending on whether the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer are parallel or anti–parallel, the electric current flowing in the first ferromagnetic barrier layer can be switched to the electric current flowing via the second ferromagnetic barrier layer between the third nonmagnetic electrode layer and the first nonmagnetic electrode layer or the electric current flowing via the same between the second nonmagnetic electrode layer and the first nonmagnetic electrode layer. The electric current flowing via the second ferromagnetic barrier layer can be controlled according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer. This corresponds to control of a collector current by a base current, as compared with the operation of a known hot electron transistor and bipolar transistor of a base ground or an emitter ground. The transistor according to this embodiment can control the current amplification factor of a collector current by a base current according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer. The transistor according to this embodiment is a transistor capable of controlling the current amplification factor and can control the collector current according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer as well as to the base current (or a bias voltage between the first and second nonmagnetic electrodes).

The coercivity of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer is changed or one of the magnetization directions is fixed. A magnetic field having a suitable strength in which any one of the directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer is inverted is applied to arbitrarily change the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer to parallel or anti-parallel. In other words, information can be stored in the transistor.

A memory cell can be constituted using the transistor. An example of a nonvolatile memory using the transistor according to this embodiment will be described below. The second nonmagnetic electrode layer of the transistor according to this embodiment is connected to a word line. The third nonmagnetic electrode layer of the transistor is connected to a bit line. The bit line is connected via a load to a power source to ground the first nonmagnetic electrode layer of the transistor. According to this structure, a specified word line is selected to apply a bias to the second nonmagnetic electrode layer. A specified bit line is selected to detect an output voltage (a voltage produced at the edge of the third nonmagnetic electrode). The output voltage is changed according to the relative directions of magnetization of the first ferromagnetic barrier layer and the second ferromagnetic barrier layer of the transistor. When the relative directions of magnetization are parallel, the output voltage is smaller. When the relative directions of magnetization are anti-parallel, the output voltage is larger. Stored information can be read depending on the magnitude of the output voltage.

In the above nonvolatile memory, the transistor according to this embodiment is used as an emitter ground transistor, the power source and load are added to the collector, and the collector voltage is an output voltage. An output voltage when the first and second ferromagnetic barrier layers have parallel magnetization by the peripheral circuits as a source voltage and load and an output voltage when they have anti-parallel magnetization can be designed to desired values. Using the above nonvolatile memory can solve the problems that the tunnel resistance is small and the output voltage is small in the MRAM using the MTJ, that the TMR ratio is small and stored information is hard to identify, and that the ratio of the output voltages is smaller by the applied bias.

The structure and operation of the transistor will be described below in detail with reference to the drawings. To easily understand the following description, the transistor according to this embodiment is called a spin filter transistor.

FIGS. 1(A) and 1(B) are diagrams showing the structure of a spin filter transistor according to this embodiment, in which FIG. 1(A) is a schematic cross-sectional view and FIG. 1(B) is an energy band diagram of conduction bands (or valence bands) of the structure shown in FIG. 1(A) with the directions of the spins of the spin bands of barrier layers. When the carriers are holes, the direction of the spin at the band edge is matched with the direction of magnetization. When the carriers are electrons, the direction of the spin at the band edge is opposite the direction of magnetization.

A spin filter transistor 1 according to this embodiment has a spin injector 5 having a first ferromagnetic barrier layer 2, a first nonmagnetic electrode layer 3 joined to one end surface of the first ferromagnetic barrier layer 2, and a second nonmagnetic electrode

layer 4 joined to the other end surface of the first ferromagnetic barrier layer 2; and a spin analyzer 8 having a second ferromagnetic barrier layer 6, the second nonmagnetic electrode layer 4 joined to one end surface of the second ferromagnetic barrier layer 6, and the third nonmagnetic electrode layer 7 joined to the other end surface of the second ferromagnetic barrier layer 6. As is apparent from FIG. 1(A), the spin injector 5 and the spin analyzer 8 share the second nonmagnetic electrode layer 4.

As the first, second and third nonmagnetic electrode layers 3, 4 and 7, a nonmagnetic metal, an n–type nonmagnetic semiconductor, or a p–type nonmagnetic semiconductor can be used. Preferably, the thickness of the second nonmagnetic electrode layer 4 is below the mean free path in the nonmagnetic electrode layer 4 of spin–polarized hot carriers injected from the spin injector. The base width is shorter than the mean free path to allow a current transmission factor to be 0.5 or above. The current amplification function can be obtained.

As the first and second ferromagnetic barrier layers 2 and 6, an insulating ferromagnetic semiconductor or a ferromagnetic insulator can be used. The energy band of the ferromagnetic barrier layer is spin split by magnetic exchange interaction. An energy region in which only an up–spin or only a down–spin exists can be formed at the band edge. The spin–polarized band is called a spin band. The energy region width is called a spin split width Δ.

As shown in FIG. 1(B), the solid lines indicated by the arrows $\uparrow$ to the ferromagnetic barrier layers 2 and 6 denote the band edges in which an up spin can exist, that is, up spin band edges 9. The solid lines indicated by the arrows $\downarrow$ thereto denote the band edges in which a down spin can exist, that is, down spin band edges 10. The portion between the up spin band edge 9 and the down spin band edge 10 in

FIG. 1(B) is a region in which only the up spin can exist. A region having an energy higher than that of the down spin band edge 10 is a region in which both the up spin and the down spin can exist. FIG. 1(B) shows the case that the spin band of the up spin is lower than the spin band of the down spin. The reverse state is also possible.

The first ferromagnetic barrier layer 2 has a thickness in which the carriers can be transmitted from the first nonmagnetic electrode layer 3 to the second nonmagnetic electrode layer 4 by the tunnel effect such as Fowler–Nordheim tunnel (hereinafter, called an FN tunnel) or direct tunnel by a voltage applied to the first nonmagnetic electrode layer 3 and the second nonmagnetic electrode layer 4. The direct tunnel refers to a phenomenon in which the carriers are directly transmitted through a thin potential barrier. The FN tunnel refers to a phenomenon in which a tunnel current by the direct tunnel can be neglected up to a certain applied voltage and the carriers are tunneled through a triangular potential in the upper portion of a potential barrier produced by applying a voltage above a certain value.

A voltage applied to the first nonmagnetic electrode layer 3 and the second nonmagnetic electrode layer 4 may be in a voltage range used in a typical memory circuit, e.g., of the order of some hundreds of mV to several V. The thickness of the second ferromagnetic barrier layer 6 must be a thickness so that thermal release of the carriers and an electric current by the tunnel (the so–called leak current) do not occur from the second nonmagnetic electrode layer 4 to the third nonmagnetic electrode layer 7.

The nonmagnetic electrode layers 3, 4 and 7 and the ferromagnetic electrode layers 2 and 6 form energy band structures shown in FIG. 1(B). Solid lines 11 of the nonmagnetic electrode layer portions in FIG. 1(B) show the Fermi energy of a metal, the Fermi

energy of an n–type (p–type) semiconductor, or the energy of the bottoms of the conduction bands (the tops of the valence bands). The lower energy barriers of the ferromagnetic barrier layers 2 and 6 to the solid lines 11 of the nonmagnetic electrode layer portions are indicated by ϕ_C and the spin split widths are indicated by Δ. The ferromagnetic barrier layers 2 and 6 may have different ϕ_C and Δ. The case that the ferromagnetic barrier layers 2 and 6 have the same ϕ_C and Δ will be shown below. When the carriers are electrons, a nonmagnetic metal or an n–type semiconductor is used as the nonmagnetic electrode layers 3, 4 and 7 and an insulating ferromagnetic semiconductor or a ferromagnetic insulator is used as the ferromagnetic barrier layers 2 and 6. In this case, the up spin band edges 9 and the down spin band edges 10 of the ferromagnetic barrier layers 2 and 6 are those in which the bottoms of the conduction bands are spin split. When the carriers are holes, a p–type semiconductor is used as the nonmagnetic electrode layers 3, 4 and 7 and an insulating ferromagnetic semiconductor or a ferromagnetic insulator is used as the ferromagnetic barrier layers 2 and 6. In this case, the up spin band edges 9 and the down spin band edges 10 of the ferromagnetic barrier layers 2 and 6 are those in which the tops of the valence bands are spin split.

The operating principle of the spin filter transistor will be described in detail. In the following description, for simplifying the description, the notation of a hot electron transistor is used together. The first nonmagnetic electrode layer 3 and the first ferromagnetic barrier layer 2 are called an emitter 21. The second nonmagnetic electrode layer 4 is called a base 22. The second ferromagnetic barrier layer 6 and the third nonmagnetic electrode layer 7 are called a collector 23. The first nonmagnetic electrode layer 3 is called the

emitter electrode 3. The third nonmagnetic electrode layer 7 is called the collector electrode 7. An example of the case that carriers are electrons will be described (when the carriers are holes, the operating principle is essentially the same and the description is omitted).

FIGS. 2(A) and 2(B) are energy band diagrams when applying base ground bias voltages between the emitter, the base, and the collector of the spin filter transistor according to this embodiment, in which FIG. 2(A) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are parallel to each other and FIG. 2(B) shows the case that the directions of magnetization of the first and second ferromagnetic barrier layers are anti-parallel to each other and corresponds to FIG. 2(A). Bias voltage V_{EB} is applied between the emitter 21 and the base 22. Bias voltage V_{CB} is applied between the base 22 and the collector 23. The magnitude of the V_{EB} is set to satisfy the relation of ($\phi_C < qV_{EB} < \phi_C + \Delta$). q is a charge quantum.

The emitter 21 serves as a spin injector injecting spin-polarized hot electrons into the base 22. When the bias voltage V_{EB} tunnel passes the carriers from the emitter electrode 3 through the first ferromagnetic barrier layer 2, the conduction band of the first ferromagnetic barrier layer 2 is spin split and the barrier heights felt by an up spin electron 24 and a down spin electron 25 existing in the emitter electrode 3 are different. In FIG. 2(A), the barrier height felt by the up-spin electron 24 is an energy to the up-spin band edge 9 of the first ferromagnetic barrier layer 2, that is, ϕ_C. The barrier height felt by the down-spin electron 25 is an energy to the down-spin band edge 10 of the first ferromagnetic barrier layer 2, that is, $\phi_C + \Delta$. Control of the base-emitter voltage can selectively tunnel inject, as a hot electron, the electron having a spin having a lower felt barrier

height, in this case, the electron 24 having an up spin into the base 22 (this phenomenon is called the spin filter effect).

The collector 23 of the spin filter transistor serves as a spin analyzer selecting the direction of the spin-polarized hot electrons injected into the base 22. A spin-polarized hot electron 26 which becomes hot by the bias voltage V_{EB} and is injected into the base 22, since the width of the base 22 is set below the mean free path of the spin-polarized hot electron 26, can ballistically arrive at the interface of the base 22 and the collector 23 without losing energy. In the second ferromagnetic barrier layer 6 of the collector 23, two barriers having different barrier heights occur by the spin split of the conduction bands. As shown in FIG. 2(A), when the directions of magnetization of the first and second ferromagnetic barrier layers 2 and 6 are parallel to each other, the up spin band edge 9 of the second ferromagnetic barrier layer 6 having a spin parallel to that of the spin-polarized hot electron 26 has an energy lower than that of the spin-polarized hot electron 26. The spin-polarized hot electron 26 is conducted to cross over the second ferromagnetic barrier layer 6 to the collector electrode 7 to be collector current I_C.

As shown in FIG. 2(B), when the directions of magnetization of the first and second ferromagnetic barrier layers 2 and 6 are anti-parallel to each other, a spin-polarized hot electron 27 having a down spin is injected into the base 22. The down spin band edge 10 of the second ferromagnetic barrier layer 6 having a down spin has an energy higher than that of the spin-polarized hot electron 27. The spin-polarized hot electron 27 cannot be conducted through the conduction band of the second ferromagnetic barrier layer 6 and is subject to spin-dependent scattering (or backscattering) at the

interface of the base 22 and the collector 23 to lose energy to become base current I_B.

The current transmission factor of an electric current flowing from the emitter to the collector is largely different depending on the relative directions of magnetization of the first ferromagnetic barrier layer 2 of the emitter 22 and the second ferromagnetic barrier layer 6 of the collector 23. In other words, the current amplification factor of the collector current by the base current is largely different.

FIGS. 3(A) and 3(B) are diagrams showing a static characteristic in the base ground of the spin filter transistor according to this embodiment in which the horizontal axis indicates collector–base voltage V_{CB} in the right direction in the drawing and emitter–base voltage V_{EB} in the left direction therein and the vertical axis indicates emitter current I_E, base current I_B, and collector current I_C, in which FIG. 3(A) shows a static characteristic of the case that the directions of magnetization of the ferromagnetic barrier layers of the emitter and the collector are parallel and FIG. 3(B) shows a static characteristic of the case that they are anti–parallel. In FIGS. 3(A) and 3(B), α is a current transmission factor, β is a current amplification factor, and the subscripts $\uparrow\uparrow$ and $\downarrow\uparrow$ indicate the case that the relative directions of magnetization of the ferromagnetic barrier layers of the emitter and the collector are parallel and the case that they are anti–parallel.

As shown in FIG. 3(A), when the directions of magnetization of the emitter and the collector are parallel, most of the emitter current I_E can be the collector current I_C. As shown in FIG. 3(B), when the directions of magnetization are anti–parallel, most of the emitter current I_E can be the base current I_B. Like a known hot electron transistor or bipolar transistor, the transistor according to this

embodiment can control the collector current I_C by the base current I_B. It can control the current amplification factor according to the relative directions of magnetization of the first and second ferromagnetic barrier layers.

As the ferromagnetic barrier layer of the spin filter transistor according to this embodiment, a ferromagnetic semiconductor such as EuS, EuSe, and EuO can be used. A ferromagnetic insulator such as $R_3Fe_5O_{12}$ (R expresses a rare–earth element) can be also used. As a nonmagnetic electrode layer, a nonmagnetic substance may be used. For instance, a metal such as Al or Au, or a nonmagnetic semiconductor such as Si or GaAs which is impurity doped with high density may be used. When EuS is used as a ferromagnetic barrier layer and Al is used as a nonmagnetic electrode layer, the barrier height Φ_C = 1.4eV and the spin split width Δ= 0.36eV. The spin filter transistor according to this embodiment can be manufactured using the above material by a known molecular beam epitaxial growth method, vacuum deposition method and sputtering method.

A nonvolatile memory using the spin filter transistor of the present invention as a memory cell will be described.

FIG. 4(A) is a diagram showing a structural example of a memory cell using the spin filter transistor 1 according to this embodiment. In the memory cell shown in FIG. 4(A), a number of spin filter transistors are arranged in matrix, emitter terminal E is grounded to connect collector terminal C and base terminal B to read bit line BL and read word line WL. A rewrite word line and a rewrite bit line are arranged to cross each other on the spin filter transistor in the state of being electrically insulated from other wires. As the rewrite word line and the rewrite bit line, the read bit line BL and the read word line WL may be used. FIG. 4(A) is a diagram showing a cell

structure of this case. In FIG. 4(A), the memory cell can be constituted by the spin filter transistor alone and can have a very simplified structure for wiring. A layout suitable for high density integration can be easily constituted. The same cell structure is used in FIG. 4(B).

A memory circuit according to this embodiment will be described with reference to FIG. 4(B). In a memory circuit 41 according to this embodiment, the second nonmagnetic electrode 4 as the base of the spin filter transistor 1 (FIG. 1) is connected to a word line 42, the third nonmagnetic electrode 7 as the collector electrode of the spin filter transistor 1 is connected to a bit line 43, the bit line 43 is connected via a load (R_L) 44 to a power source (V_{CC}) 45, and the first nonmagnetic electrode 3 as the emitter electrode of the spin filter transistor 1 is grounded. A pure resistance is used as the load. An active load by the transistor may be used.

To read stored information of a specified memory cell, the specified word line 42 is selected to apply a bias between the emitter and the base, the source voltage V_{CC} of the power source 45 is applied via the load resistance 44 to the bit line 43, the stored information is read according to the magnitude of output voltage V_O appearing on the bit line 43. In FIG. 4(C), the vertical axis indicates collector current I_C, the horizontal axis indicates collector–emitter voltage V_{CE}, and an I_C–V_{CE} characteristic of the spin filter transistor and a load straight line 46 by the load resistance 44 are shown in the same drawing.

The output voltage V_O is determined from the crossing point of these characteristics. Output voltages in which the mutual magnetization states of the first and second ferromagnetic barrier layers 2 and 6 are parallel and anti–parallel are $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$, as shown in FIG. 4(C). The absolute values of the $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$ and the

ratio of the $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$ can be optimized by the circuit parameters (R_L and V_{CC}). The nonvolatile memory device according to this embodiment can obtain output signals having a necessary magnitude and the ratio of output signals without adjusting the structure of the device itself unlike the MTJ.

The spin filter effect used in the transistor according to this embodiment is an effect using the spin split of the bands of the ferromagnetic substances and has a spin selectivity higher than that of the TMR effect of the MTJ. When the base width is set below the mean free path of the spin–polarized hot carriers and the relative magnetization state between the first and second ferromagnetic barrier layers is parallel magnetization, the current transmission factor α (defined by = I_C / I_E) can be 0.5 or above. When it is anti–parallel magnetization, the current transmission factor is very small. The change in the current transmission factor in the case of parallel magnetization and anti–parallel magnetization is further amplified, seen from the current amplification factor β (defined by = I_E / I_B). The above peripheral circuits optimize the output signal to the output characteristic of the spin filter transistor which is largely different in the magnetization state. The desired absolute values of output signals and the desired ratio of output signals can be easily obtained.

A nonvolatile memory circuit using the transistor having an output characteristic depending on the direction of the spin of carriers (hereinafter, called a "spin transistor") will be described.

The memory circuit according to the present invention relates to a nonvolatile memory circuit using the spin transistor. The spin transistor includes ferromagnetic substances such as a ferromagnetic metal and a ferromagnetic semiconductor and controls the direction of

the spin of carriers according to the magnetization state to change the output characteristic. Information is stored based on the magnetization state of the ferromagnetic substances in the spin transistor. The output characteristic of the transistor reflecting the magnetization state in the spin transistor is used to read the information. A one-bit nonvolatile memory cell can be constituted by one spin transistor. The values of output signals to the stored information can be optimized by the peripheral circuits connected to the memory cell.

In greater detail, the spin transistor has at least one ferromagnetic layer (free layer) capable of independently controlling the direction of magnetization by a magnetic field and at least one ferromagnetic layer (pin layer) in which the direction of magnetization is fixed or having a coercivity larger than that of the free layer and is a transistor capable of controlling the output characteristic of the transistor according to the relative directions of magnetization of the free layer and the pin layer under the same bias. The direction of magnetization of the free layer is changed by a magnetic field. The relative magnetization states of the free layer and the pin layer can be two states of parallel magnetization and anti-parallel magnetization. The two magnetization states correspond to binary stored information.

The spin transistor can obtain the output characteristic according to the magnetization state in the transistor based on a conductive phenomenon changed depending on the direction of the spin of carriers such as spin-dependent scattering, tunneling magnetoresistance effect, and spin filter effect. The spin transistor has a first electrode structure injecting spin-polarized carriers, a second electrode structure receiving the spin-polarized carriers, and

a third electrode structure controlling the amount of the spin-polarized carriers conducted from the first electrode structure to the second electrode structure.

The spin transistor is operated based on the same operating principle as a typical transistor other than the conductive phenomenon depending on the spin. The spin transistor can be classified as a current-driven type transistor such as a bipolar transistor or a voltage-driven type transistor such as an electric field effect transistor. In the current-driven type transistor, the first electrode structure corresponds to an emitter, the second electrode structure corresponds to a collector, and the third electrode structure corresponds to a base. The spin filter transistor described in this embodiment is classified as the current-driven type. In the voltage-driven type transistor, the first electrode structure corresponds to the source, the second electrode structure corresponds to the drain, and the third electrode structure corresponds to the gate. The output current (collector current or drain current) in the spin transistor is changed according to the magnetization state of the ferromagnetic substances included in the spin transistor under the same bias.

The detail of the spin transistor will be described later. Typical output characteristics of spin transistors and a nonvolatile memory using the spin transistors will be described. A magnetic field is applied to the free layer in the spin transistor to make it possible to realize parallel magnetization or anti-parallel magnetization of the relative magnetization state of the free layer and the pin layer. The magnetization state can stably exist unless a magnetic field above the coercivity of the free layer is applied.

FIG. 5(A) schematically shows an example of an output characteristic of the current–driven type spin transistor. Like a typical current–driven type transistor, the collector current I_C can be controlled according to the magnitude of the base current I_B. The magnitude of the collector current depends on the magnetization state of the ferromagnetic substance included in the spin transistor. In FIG. 5(A), when applying the same bias to the spin transistor ($I_B = I_{B1}$), the collector current $I_{C\uparrow\uparrow}$ is large in parallel magnetization and the collector current $I_{C\downarrow\uparrow}$ is small in anti–parallel magnetization.

FIG. 5(B) schematically shows an example of an output characteristic of the voltage–driven type spin transistor. Like a field–effect transistor such as a typical MOS transistor, when a gate–source voltage (V_{GS}) is smaller than threshold value V_T ($V_{GS} < V_T$), the spin transistor is in the non–conductive state and a drain current is hardly produced. When applying the V_{GS} above the V_T, the spin transistor is brought to the conductive state. Under the same bias ($V_{GS} = V_{GS1}$), when the ferromagnetic substance included in the spin transistor has parallel magnetization or anti–parallel magnetization, a drain current value is different. In FIG. 3(B), in the case that it has parallel magnetization, the drain current $I_{D\uparrow\uparrow}$ is large, and in the case that it has anti–parallel magnetization, the drain current $I_{D\downarrow\uparrow}$ is small.

The spin transistor can electrically detect the relative directions of magnetization of the free layer and the pin layer included in the devices of the current–driven type and the voltage–driven type based on the magnitude of the collector current or the drain current. As described above, the ferromagnetic substances can stably hold the direction of magnetization unless a magnetic field above the coercivity of the free layer from outside is applied. The spin transistor can store, in nonvolatile manner, binary

information by allowing the relative magnetization state of the free layer and the pin layer included in the device to be parallel magnetization or anti-parallel magnetization. A one-bit nonvolatile memory cell can be constituted only by one spin transistor.

Taking the case of using the voltage-driven type spin transistors as an example, a nonvolatile memory using the spin transistors will be described below in detail. A nonvolatile memory using the current-driven type spin transistors as memory cells can be constituted in the same manner.

FIG. 6(A) is a diagram showing a structural example of memory cells using spin transistors. FIG. 6(B) is a diagram snowing a structural example of a memory circuit formed based on the memory cells. The relation of FIGS. 6(A) and 6(B) is the same as that of FIGS. 4(A) and 4(B). In the memory cell shown in FIG. 6(A), a number of spin transistors 150 are arrayed in matrix, and source S is grounded to connect drain D and gate G to read bit line BL and read word line WL, respectively. A rewrite word line and a rewrite bit line are arranged to cross each other on the spin transistor 150 in the state of being electrically insulated from other wires. As the rewrite word line and the rewrite bit line, the read bit line BL and the read word line WL may be used. FIGS. 6(A) and 6(B) are diagrams showing the structure of this case. In FIGS. 6(A) and 6(B), the memory cell can be constituted by one spin transistor and can have a very simplified structure for wiring.

In particular, in the voltage-driven type spin transistor having a form similar to that of a MOS transistor, the source is shared between adjacent memory cells. A layout suitable for microfabrication can be easily constituted.

The rewrite/read bit line and rewrite/read word line are simply called bit line BL and word line WL.

Information is rewritten by flowing electric currents to the bit line BL and the word line WL crossing on the selected memory cell to invert the free layer of the selected memory cell by a synthesized magnetic field induced by the electric currents flowing to the respective wires. In this case, in order that the non-selected cell connected to the same bit line BL or word line WL as those of the selected cell is not magnetization inverted, current values flowing to the respective wires are set so that magnetization inversion does not occur in the magnetic field from one of the wires.

In reading information, a voltage is applied to the word line WL connected to the selected cell to conduct the spin transistor, and then a voltage is applied to the bit line to detect the magnitude of a drain current. Based on the magnitude of the drain current, the relative magnetization state of the free layer and the pin layer can be detected.

FIG. 6(B) is a memory circuit connected to output terminal V_O and source voltage V_{DD} branched from the output terminal V_O via a load to the bit line end of the memory circuit shown in FIG. 6(A). FIG. 6(C) shows a static characteristic and operating points of the memory cell shown in FIG. 6(B). Here, an active load 160 by a depression type MOS transistor is used as the load. A pure resistance may be used, as shown in FIG. 4(B). As shown in FIG. 6(C), gate voltage V_{GS} is applied to the gate of the spin transistor 150 at reading information to apply the source voltage V_{DD} via the load to the bit line BL. The operating points by the active load are moved on the load curve in FIG. 6(C) according to the magnetization state of the pin layer and the free layer (P11 and P12 in the drawing). The output signals V_O in parallel magnetization and anti-parallel magnetization are $V_{O\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$ in

the drawing. The absolute values and the ratio of ($V_{O\uparrow\uparrow}/V_{O\downarrow\uparrow}$) of the respective output signals can be optimized by a transistor characteristic of the active load and the parameters of the peripheral circuits such as V_{DD}. For instance, the cross point of the static characteristic of the spin transistor and the load curve by the active load is optimized. When drain current ratio $I_{O\uparrow\uparrow}/I_{O\downarrow\uparrow}$ is small, a large output signal ratio can be obtained. When the values of $I_{O\uparrow\uparrow}$ and $I_{O\downarrow\uparrow}$ are varied by the memory cell and the saturation current of the active load is larger than $I_{O\downarrow\uparrow}$ and is smaller than $I_{C\uparrow\uparrow}$, the output voltage can be hardly changed. Since no sense amp is used for reading information, high-speed reading is possible. The memory circuit of this embodiment has the advantages that an output signal having a desired magnitude can be easily obtained and that high-speed read is possible.

In the memory cell using the prior art MTJ and MOS transistor, an output voltage according to the resistance of the MTJ is read by a sense amp. The output voltage is determined by a current value flowing to the MTJ and an impedance (junction resistance) of the MTJ. The output voltage ratio cannot be freely adjusted by the peripheral circuits.

The structure of a spin transistor applicable to the nonvolatile memory circuit according to this embodiment will be described with reference to the drawings. FM is an abbreviation of a ferromagnetic metal, FS is an abbreviation of an electrically conductive ferromagnetic semiconductor, IFS is an abbreviation of an insulating ferromagnetic semiconductor, and NM is an abbreviation of a nonmagnetic substance. An NM metal denotes a nonmagnetic metal, and an NM semiconductor denotes a nonmagnetic semiconductor. The current-driven type spin transistors will be described.

FIG. 7 is an energy band diagram of a hot electron transistor type spin transistor. A spin transistor 200 has an emitter 201 and a base 205 made of FM or FS. In greater detail, the spin transistor 200 has the emitter 201 made of FM (or FS), an emitter barrier 203 made of NM, the base 205 made of FM (or FS), a collector barrier 207 made of NM, and a collector 211 made of NM. As the NM, a nonmagnetic metal or a nonmagnetic semiconductor can be used.

In the spin transistor 200 shown in FIG. 7, spin–polarized hot carriers are tunnel injected from the emitter 201 via the emitter barrier 203 to the base 205.

When the emitter 201 and the base 205 have parallel magnetization, the injected spin–polarized hot carriers are hardly subject to spin–dependent scattering in the base 205. When a base width is set so that the spin–polarized hot carriers can be ballistically transmitted through the base 205, they cross over the collector barrier 207 to the collector 211. The same transistor operation as that of a typical hot electron transistor is performed.

When the emitter 201 and the base 205 have anti–parallel magnetization, the spin–polarized hot carriers injected from the emitter 201 into the base 205 lose energy by the spin–dependent scattering in the base 205 to be a base current without crossing over the collector barrier 207. When the emitter 201 and the base 205 have anti–parallel magnetization, the current transmission factor is lower than the case that both have parallel magnetization. When applying the same bias to the spin transistor 200, the difference in the relative magnetization state of the emitter 201 and the base 205 makes the current transmission factor or the current amplification factor different. The spin transistor 200 can be operated at room temperature by suitably selecting the barrier height of the collector barrier.

The spin transistor 200 must have a large base width so that the spin-dependent scattering can effectively function to increase the ratio of the current transmission factors in the case that the emitter and the base have parallel magnetization and the case that they have anti-parallel magnetization. When the base width is increased and the emitter and the base have parallel magnetization, the current transmission factor is smaller and is below 0.5 so that a trade-off in which the amplification function is lost exists.

FIG. 8 is an energy band diagram of a hot electron transistor type spin transistor using thermal release as a spin injection mechanism to a base. As shown in FIG. 8, a spin transistor 220 has an emitter 221 made of FM (or FS), a base 225 made of FM (or FS), and an emitter barrier 223 made of NM provided between both. It further has a collector barrier 227 of NM, and a collector 231 of NM on the opposite side of the junction of the base 225 and the emitter barrier 223. A nonmagnetic semiconductor can be used for the emitter barrier 223 and the collector barrier 227. A nonmagnetic semiconductor or a nonmagnetic metal can be used for the collector 231.

An ohmic contact or a tunnel contact is formed between the emitter 221 and the emitter barrier 223. A junction is formed between the base 225 and the emitter barrier 223 or between the base 225 and the collector barrier 227 so as to have band discontinuity shown in FIG. 9. The band discontinuity can be realized by a Schottky junction between the NM semiconductor and FM and a heterojunction between the NM semiconductor and FS. Alternatively, a Schottky junction is formed of FS and FM, a Schottky barrier produced in this case is an emitter barrier, FS is an emitter, and FM is a base.

The spin-polarized carriers diffused from the emitter 221 to the emitter barrier 223 by applying a bias to the base 225 with respect to

the emitter 221 are injected as hot carriers into the base 225 by thermal release. When the emitter 221 and the base 225 have parallel magnetization, the spin-polarized carriers injected into the base 225 can reach the collector without being subject to spin-dependent scattering. When the emitter 221 and the base 225 have anti-parallel magnetization, the spin-polarized hot carriers become a base current by spin-dependent scattering. The spin transistor 220 uses spin-dependent scattering in the base. Like the spin transistor 200, a trade-off relation exists between the ratio of the current transmission factors in parallel magnetization and anti-parallel magnetization and the current transmission factor in parallel magnetization. As compared with the spin transistor 200 using tunnel injection, there are characteristics that a current driving force can be large and that room-temperature operation can be easily realized.

FIG. 9 is an energy band diagram of a hot electron transistor type spin transistor using the spin filter effect. Although the transistor is already described in detail, its characteristic will be briefly described. A spin transistor 240 shown in FIG. 9 has an emitter barrier 243 and a collector barrier 247 made of IFS. From an emitter 241 made of an NM semiconductor (or NM metal), only carriers having one of spins by the spin filter effect of the emitter barrier 243 can be selectively injected into a base 245 made of an NM semiconductor (or NM metal). The base width is set below the mean free path of the spin-polarized hot carriers. The spin-polarized hot carriers injected into the base 245 are ballistically conducted through the base 245. At this time, the spin transistor 240 is biased so that the spin-polarized hot carriers are injected into the energy split width of the up spin band of the collector barrier 247 (the spin band edge indicated by the upward arrow in FIG. 9) and the down spin band (the spin band edge

indicated by the downward arrow in FIG. 9). When the emitter barrier 243 and the collector barrier 247 have parallel magnetization, the spin-polarized hot carriers injected into the base 245 cross over the barrier by the spin band having a low energy in the collector barrier 247 by the spin filter effect of the collector barrier 247 and can be propagated to a collector 251 of an NM semiconductor (or NM metal). When the emitter barrier 243 and the collector barrier 247 have anti-parallel magnetization, most of the spin-polarized hot carriers become a base current without crossing over the collector barrier 247 by the spin filter effect of the collector barrier 247.

In the spin transistor 240, the current transmission factor (or current amplification factor) is different according to the relative directions of magnetization of the emitter barrier 243 and the collector barrier 247. The spin filter effect has a very large spin selectivity. The ratio of the current transmission factors in parallel magnetization and anti-parallel magnetization can be increased in the transistor.

The spin transistor 240 can sufficiently decrease the base width. Unlike the spin transistor using spin-dependent scattering shown in FIGS. 7 and 8, there is the advantage that a trade-off related to the base width between the current amplification factor and the spin selectivity does not exist.

FIG. 10 is an energy band diagram of a tunnel base transistor type spin transistor. As shown in FIG. 10, in a tunnel base transistor type spin transistor 260, a p-type (or n-type) FS is used for an emitter 261 and a collector 265 and an n-type (or p-type) NM semiconductor is used for a tunnel base 263. It is preferable to use a heterojunction of type II so that the base 263 is a barrier to holes (or electrons) between the emitter and the base and between the base and the

collector. The base width is smaller so as to produce a tunnel current from the emitter to the collector.

In the structure shown in FIG. 10, when the emitter 261 and the collector 265 have parallel magnetization, carriers having a number of spins of the emitter can be easily tunneled to the collector 265 and the tunnel conductance is large. When the emitter 261 and the collector 265 have anti-parallel magnetization, the tunnel conductance is small by the tunneling magnetoresistance effect (TMR effect). The magnitude of the collector current can be controlled according to the relative magnetization state of the emitter 261 and the collector 265.

When the TMR ratio in the spin transistor 260 can be large, the change in the collector current depending on the magnetization state of the emitter and the collector can be increased. To effectively exhibit the TMR effect by the spin transistor 260, preferably, a depression layer is not expanded to the collector side when applying a reverse bias to the base-collector junction. When the depression layer is expanded to the base side, the possibility that a problem arises in the saturation characteristic of the collector current exists.

When the base layer is doped with high density so as not to expand the depression layer to the base layer in the spin transistor 260 and the depression layer of the base-collector junction is expanded to the collector side, the TMR effect in the base cannot be expected and the carriers injected into the collector produce resistance by spin-dependent scattering in the collector. Using the spin-dependent scattering can change the magnitude of the collector current according to the magnetization state of the emitter and the collector. The change in resistance by the spin-dependent scattering is small. As compared with using the TMR effect, the effect may be not high.

The voltage–driven type spin transistors will be described with reference to the drawings.

FIG. 11 is a diagram showing the cross–sectional structure of a MOS transistor type spin transistor. As shown in FIG. 11, a MOS transistor type spin transistor 300 has a structure in which a source 303 made of FM, a drain 305 made of FM, and a gate electrode 311 via a gate insulator film 307 are formed on an NM semiconductor 301. A Schottky junction of the FM and NM semiconductor is used for the source 303 and the drain 305. Other structure is the same as that of a typical MOS transistor.

Spin–polarized carriers injected from the source 303 into a channel formed directly below the gate insulator film 307 in the NM semiconductor 301 pass through the channel to the drain 305 (hereinafter, for simplification, the influence of the Rashba effect by the gate electric field of the spins injected into the channel is neglected). When the source 303 and the drain 305 have parallel magnetization, the spin–polarized carriers injected into the drain 305 are not subject to spin–dependent scattering. When they have anti–parallel magnetization, resistance by spin–dependent scattering is produced in the drain electrode 305.

In the transistor 300, the mutual conductance is different according to the relative directions of magnetization of the source and the drain.

FS can be also used for the source 303 and the drain 305 to form a pn junction between it and the semiconductor 301 to form a source and a drain.

FIG. 12 is a diagram showing the cross–sectional structure of a modulation dope transistor type spin transistor. A spin transistor 320 has a source 323 made of FM (or FS) to a two–dimensional carrier gas

produced at the interface of a first NM semiconductor 321 and a second NM semiconductor 327, a drain 325 made of FM (or FS), and a gate electrode 331. It is the same as a typical modulation dope transistor except that the source 323 and the drain 325 are made of ferromagnetic substances.

Spin–polarized carriers are injected from the source 323 into a channel 333 formed by the two–dimensional carrier gas. The spin–polarized carriers which have reached the drain 325 have different mutual conductance according to the relative directions of magnetization of the source 323 and the drain 325 due to spin–dependent scattering in the drain 325.

FIG. 13 is a cross–sectional view of a MOS transistor type spin transistor using FS for a channel region. A spin transistor 340 shown in FIG. 13 has a structure in which a source 343 made of FM, a drain 345 made of NM (or FM or FS) and a gate electrode 351 via a gate insulator film 347 are formed on an FS 341. A Schottky junction of the FM and FS is used for the source 343. Other structure is the same as that of a typical MOS transistor.

Spin–polarized carriers are tunnel injected from the source 343 via the Schottky barrier into the channel 341. The mutual conductance depending on the relative directions of magnetization of the source 343 and the FS 341 is realized by the TMR effect at the tunnel injection and spin–dependent scattering in the channel of the FS 341.

A spin transistor 360 showing its cross–sectional structure in FIG. 14 is a spin transistor having a tunnel junction structure interposing an insulating NM tunnel barrier 365 between a source 361 made of FM (FS) and a drain 363 made of FM (or FS) and arranging a gate electrode 371 so as to apply an electric field to the tunnel barrier 365.

The film thickness of the tunnel barrier 365 is preferably set to a thickness so that no Fowler–Nordheim (FN) tunnel occurs when applying only a bias between the source and the drain. The triangular potential of the tunnel barrier band edge produced by applying a bias between the source and the drain is changed by a gate voltage to induce the FN tunnel to obtain a drain current.

Spin–polarized carriers injected from the source 361 are subject to spin–dependent scattering in the drain 363 according to the relative magnetization state of the source 361 and the drain 363. The mutual conductance of the transistor can be controlled by the relative directions of magnetization of the source and the drain.

A spin transistor 380 showing its cross–sectional structure in FIG. 15 replaces the tunnel barrier of the spin transistor 360 shown in FIG. 14 with a tunnel barrier 385 made of IFS. A source 381 must be of FM or FS. A drain 383 need not be a ferromagnetic substance. The barrier height of the IFS tunnel barrier layer 385 is different according to the direction of the spin of carriers. When the source 381 and the tunnel barrier 385 have parallel magnetization, a bias is applied between the source and the drain and between the source and the gate so that the transistor is brought to the conductive state. Under the same bias condition, when the source 381 and the tunnel barrier 385 have anti–parallel magnetization, the height of the tunnel barrier seen from a number of spins of the source 381 is increased. The tunnel probability of the spin–polarized carriers is decreased to reduce the drain current. The spin selectivity by the spin filter effect is very large. When using a ferromagnetic substance having a large spin polarizability as the source 381, the mutual conductance according to the relative directions of magnetization of the source and the drain can be largely changed.

The above-described various spin transistors can be used as the memory cells for the memory circuit shown in FIG. 4 or FIG. 6.

It is also possible to form a structure in which the sources of the two voltage-driven type spin transistors shown in FIGS. 11, 14 and 15 are shared as one source. FIG. 16(A) is a diagram showing a structural example of memory cells having a shared source structure. FIG. 16(B) is a diagram showing a cross-sectional structural example of the memory cells having a shared source structure.

The memory cell structure shown in FIGS. 16(A) and 16(B) has first spin transistor Tr1 and second spin transistor Tr2 adjacent each other, word line WL sharably connecting gate electrode G1 of the first spin transistor Tr1 and gate electrode G2 of the second spin transistor Tr2, first bit line BL1 connected to first drain D1 of the first spin transistor Tr1, second bit line BL2 connected to second drain D2 of the second spin transistor, ferromagnetic source S shared between the first and second spin transistors Tr1 and Tr2, and a wire grounding it. Using the above structure shares the source provides a cell structure suitable for high density integration.

To minimize a leak current at non-conduction, in the voltage-driven type spin transistors shown in FIGS. 11, 14 and 15, it is preferable to use an SOI substrate having a high insulation, as shown in FIG. 16(B).

As described above, the spin filter transistor according to the embodiments of the present invention and various spin transistors shown in this embodiment have a characteristic capable of controlling an output characteristic according to the relative directions of magnetization of the pin layer and the free layer included in the device. The relative magnetization state has a nonvolatile characteristic capable of holding the state without supplying an

electric power. The relative magnetization states can be stored as binary information in nonvolatile manner. Using the above output characteristic can electrically detect the relative magnetization state. A one-bit nonvolatile memory cell can be constituted only by one spin transistor. Using the nonvolatile memory circuit using the spin transistor according to this embodiment can freely design the magnitude of output signals and the ratio of output signals to stored information.

Using the spin transistor according to this embodiment of the present invention and a memory circuit using the same can increase the operating speed and integration of the nonvolatile memory circuit.

The present invention is described above along the embodiments. The present invention is not limited to these. It is apparent to those skilled in the art that various modifications, improvements and combinations can be made.

INDUSTRIAL APPLICABILITY

As described above, the spin filter transistor of the present invention can largely change an output characteristic according to the relative directions of magnetization of ferromagnetic barrier layers.

The nonvolatile memory circuit using, as memory cells, the spin filter transistor and another spin transistor having a characteristic equal to that of this can store binary information according to the relative directions of magnetization of ferromagnetic substances included in the transistor and can electrically detect the relative directions of magnetization. Using the nonvolatile memory circuit of the present invention can freely design output signals to stored information. A high-speed nonvolatile memory circuit with high

density integration constituting a one-bit nonvolatile memory cell only by one transistor can be realized.